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NOTICE OF ALLOWANCE AND FEE(S) DUE

23353 7590 11/18/2008

RADER FISHMAN & GRAUER PLLC
LION BUILDING
1233 20TH STREET N.W., SUITE 501
WASHINGTON, DC 20036

EXAMINER	
GANDHI, DIPAKKUMAR B	
ART UNIT	PAPER NUMBER
2117	

DATE MAILED: 11/18/2008

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/647,217	08/26/2003	Yoshitaka Kayukawa	SON-2810	1901

TITLE OF INVENTION: SEMICONDUCTOR INTEGRATED CIRCUIT AND METHOD FOR TESTING SAME

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	02/18/2009

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
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INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

23353 7590 11/18/2008

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Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/647,217	08/26/2003	Yoshitaka Kayukawa	SON-2810	1901

TITLE OF INVENTION: SEMICONDUCTOR INTEGRATED CIRCUIT AND METHOD FOR TESTING SAME

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	02/18/2009

EXAMINER	ART UNIT	CLASS-SUBCLASS
GANDHI, DIPAKKUMAR B	2117	714-727000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

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This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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GANDHI, DIPAKKUMAR B	
ART UNIT	PAPER NUMBER
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DATE MAILED: 11/18/2008

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 301 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 301 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

Notice of Allowability	Application No.	Applicant(s)	
	10/647,217	KAYUKAWA ET AL.	
	Examiner	Art Unit	
	DIPAKKUMAR GANDHI	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *08/06/2008*.

2. ☒ The allowed claim(s) is/are *24-30, 32, 33, 35-44, which are renumbered as 1-19*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/Cynthia Britt/
Primary Examiner, Art Unit 2117

Allowable Subject Matter

1. Claims 24-30, 32, 33, 35-44 are allowed.

2. Claims 1-23, 31, 34 are cancelled.

3. Applicants' amendment including amended claims filed on 08/06/2008 has been entered.

4. The 35 U.S.C. 112, second paragraph rejection for claims 24-30, 32-33 and 35 is withdrawn.

5. The following is an examiner's statement of reasons for allowance:

The present invention relates to a semiconductor integrated circuit, such as an LSI, and relates particularly to a semiconductor integrated circuit in which a scan circuit is provided, as well as a method of testing same.

The claimed invention in claim 24 recites features such as:"…a reset means for resetting said plurality of flip-flops at a transition time, between said test mode and said normal mode, responsive to a scan mode signal for selectively specifying one of said normal operation mode and said test mode by the logical level of said mode signal, whereby said resetting is always performed at said transition time."

The prior art of record (Hashizume US 6,539,511 B1) teaches in a semiconductor integrated circuit device supporting a boundary scan test, the state of an I/O cell is set under the control of a DC test control circuit through a boundary scan register utilized for the boundary scan test for setting an external terminal connected with a pad in a desired state. A semiconductor integrated circuit device allowing execution of a DC test without increasing the circuit area and signal propagation delay is provided (abstract, Hashizume).

Cavaliere et al. (US 3,961,254) teach an LSI semiconductor device includes a memory array incorporating address, data and buffer registers, and associated combinatorial and/or sequential logic circuitry. The array is "embedded" in the sense that the memory array is not directly accessible, either in whole or in part, from the input and output terminals or pads of the device. To facilitate testing, means which bypass the associated logic circuitry are provided for scanning information directly into the address and data registers (abstract, Cavaliere et al.).

Tamamura et al. (US 6,118,316) teach a semiconductor integrated circuit generating a stabilized oscillation signal based on an input signal includes a plurality of unit circuits connected in series, each of

the unit circuits having at least an oscillator, a divider, and a phase comparator which construct at least one part of a phase-locked loop. In the unit circuit, a frequency of an oscillation output signal of a latter one of the unit circuits is higher than that of an oscillation output signal of a former one of the unit circuits (abstract, Tamamura et al.).

Bae et al. (KR 2001011641 A) teach an apparatus comprises an input buffer(10) for taking as an input a source clock signal and converting the external TTL level into CMOS level; a rising edge detection unit(20) for detecting the rising edge of a source clock signal(clock); a falling edge detection unit(30) for detecting the falling edge of the source clock signal; and an internal clock signal generating unit(40) for outputting an internal test clock signal(iclkp) synchronized with the rising edge and the falling edge of the source clock signal, respectively, during a high speed operation test mode of the semiconductor device (abstract, Bae et al.).

The prior arts however do not teach a reset means for resetting said plurality of flip-flops at a transition time, between said test mode and said normal mode, responsive to a scan mode signal for selectively specifying one of said normal operation mode and said test mode by the logical level of said mode signal, whereby said resetting is always performed at said transition time.

Hence, the prior arts of record do not anticipate nor render obvious the claimed invention. Thus, claim 24 is allowable over the prior arts of record. Claims 25-30, 32, 33 and 35 are allowed because of the combination of additional limitations and the limitations listed above.

- The claimed invention in claim 36 recites features such as:"…a reset means for resetting said plurality of flip-flops at a transition time, between said test mode and said normal mode, responsive to said scan mode signal for selectively specifying one of said normal operation mode and said test mode by the logical level of said mode signal, wherein said reset means is responsive to a reset signal inputted from a reset input terminal and resets said plurality of flip-flops at said transition time, between said test mode and said normal mode, in accordance with said mode signal."

The prior art of record (Hashizume, US 6,539,511 B1) teaches that in a semiconductor integrated circuit device supporting a boundary scan test, the state of an I/O cell is set under the control of a DC test

control circuit through a boundary scan register utilized for the boundary scan test for setting an external terminal connected with a pad in a desired state (abstract, Hashizume).

Naitoh et al. (US 5,040,150) teach a semiconductor integrated circuit device comprising a first circuit forming a random logic and outputting a plurality of first parallel data of plural bits, a second circuit which receives the plurality of first parallel data and supplies a plurality of second parallel data of plural bits to the first circuit, and a test circuit which divides a part of external parallel data of plural bits smaller in number than the first parallel data into a plurality of third parallel data of plural bits in such a manner that the plurality of third parallel data correspond in number to the plurality of first parallel data (abstract, Naitoh et al.).

Cavaliere et al. (US 3,961,254) teach an LSI semiconductor device includes a memory array incorporating address, data and buffer registers, and associated combinatorial and/or sequential logic circuitry. The array is "embedded" in the sense that the memory array is not directly accessible, either in whole or in part, from the input and output terminals or pads of the device. To facilitate testing, means which bypass the associated logic circuitry are provided for scanning information directly into the address and data registers. The information so introduced is shifted through the register strings. The interconnections from the associated logic circuitry are inhibited during the testing mode while the information shifting means are inhibited during an operative mode. The information scanned into the registers may be scanned out to determine whether there is a defect or problem in the register strings. Output levels from the array are compared with an expected output (abstract, Cavaliere et al.).

Tamamura et al. (US 6,118,316) teach a semiconductor integrated circuit generating a stabilized oscillation signal based on an input signal includes a plurality of unit circuits connected in series, each of the unit circuits having at least an oscillator, a divider, and a phase comparator which construct at least one part of a phase-locked loop. In the unit circuit, a frequency of an oscillation output signal of a latter one of the unit circuits is higher than that of an oscillation output signal of a former one of the unit circuits (abstract, Tamamura et al.).

Bae et al. (KR 2001011641 A) teach that an internal clock generating apparatus is provided to reduce test time by generating internal test clock pulses synchronized with both the rising and falling edges of a source clock signal, respectively (abstract, Bae et al.).

DeLisle et al. (US 5,283,889) teach that a relatively fast system control processor, such as an Intel 8051, is substituted for an Intel 8042 microprocessor in a PC/AT type compatible personal computer. In one embodiment of the invention, a System Control Processor Interface (SCPI) is provided between the central processing unit (CPU) and the system control processor (SCP) to maintain compatibility with the PC/AT bus. The combination of the faster SCP and the SCPI interface improves the overall system performance. Control circuitry is also provided for setting the A20 signal relatively quickly to allow memory access above one megabyte (abstract, DeLisle et al.).

Yutaka (JP 63134970) teaches that design data of an IC 10 consisting of a logic circuit group before inserting a scan latch is read from a fundamental data holding part 11, and the confirmation facility of existence of a fault in an input end and an output end of a circuit is calculated by a fault existence confirmation facility calculating part 12. Also, by a control facility calculating part 13, the setting facility of a signal to the input end for confirming a fault is calculated. Subsequently, their rank order is discriminated by rank order discriminating parts 14, 15, and in order from that which is inferior inconfirmation facility, and that which is inferior in control facility, a write/read scanning circuit is inserted, and FFs 1 W8 become scan FFs. In this state, a regular scan test and a non-scan test are executed (abstract, Yutaka).

Ichiro (JP 04287510) teaches a usual flip-flop 17 acts like a usual flip-flop when an MD is zero and a scanning flip-flop 18 reaches the data load state. When the MD is '1', the scanning flip-flop 18 acts like a usual flip-flop and the usual flip-flop 17 reaches the data load state, then each clock is made independent. The test of the circuit by scanning is executed independently of the kind and state of a system clock signal (abstract, Ichiro).

The prior arts however do not teach a reset means for resetting said plurality of flip-flops at a transition time, between said test mode and said normal mode, responsive to said scan mode signal for selectively specifying one of said normal operation mode and said test mode by the logical level of said mode signal,

wherein said reset means is responsive to a reset signal inputted from a reset input terminal and resets said plurality of flip-flops at said transition time, between said test mode and said normal mode, in accordance with said mode signal.

Hence the prior arts of record do not anticipate nor render obvious the claimed invention. Thus, claim 36 is allowable over the prior arts of record. Claims 37-40 are allowed because of the combination of additional limitations and the limitations listed above.

- The claimed invention in claim 41 recites features such as:"…a reset input signal for controlling reset of said flip-flops by a reset control block provided to detect a transition time of a logical level of the scan mode signal by an edge detection signal having a pulse length that is at least equal to or greater than one clock period of a system clock, wherein scan operations are inhibited without resetting at the time of initiating scan operations or normal operations without being reset upon termination of scan operations, whereby said resetting is always performed at said transition time."

The prior art of record (Hashizume, US 6,539,511 B1) teaches that in a semiconductor integrated circuit device supporting a boundary scan test, the state of an I/O cell is set under the control of a DC test control circuit through a boundary scan register utilized for the boundary scan test for setting an external terminal connected with a pad in a desired state (abstract, Hashizume).

Naitoh et al. (US 5,040,150) teach a semiconductor integrated circuit device comprising a first circuit forming a random logic and outputting a plurality of first parallel data of plural bits, a second circuit which receives the plurality of first parallel data and supplies a plurality of second parallel data of plural bits to the first circuit, and a test circuit which divides a part of external parallel data of plural bits smaller in number than the first parallel data into a plurality of third parallel data of plural bits in such a manner that the plurality of third parallel data correspond in number to the plurality of first parallel data (abstract, Naitoh et al.).

Cavaliere et al. (US 3,961,254) teach an LSI semiconductor device includes a memory array incorporating address, data and buffer registers, and associated combinatorial and/or sequential logic circuitry. The array is "embedded" in the sense that the memory array is not directly accessible, either in

whole or in part, from the input and output terminals or pads of the device. To facilitate testing, means which bypass the associated logic circuitry are provided for scanning information directly into the address and data registers. The information so introduced is shifted through the register strings. The interconnections from the associated logic circuitry are inhibited during the testing mode while the information shifting means are inhibited during an operative mode. The information scanned into the registers may be scanned out to determine whether there is a defect or problem in the register strings. Output levels from the array are compared with an expected output (abstract, Cavaliere et al.).

Tamamura et al. (US 6,118,316) teach a semiconductor integrated circuit generating a stabilized oscillation signal based on an input signal includes a plurality of unit circuits connected in series, each of the unit circuits having at least an oscillator, a divider, and a phase comparator which construct at least one part of a phase-locked loop. In the unit circuit, a frequency of an oscillation output signal of a latter one of the unit circuits is higher than that of an oscillation output signal of a former one of the unit circuits (abstract, Tamamura et al.).

Bae et al. (KR 2001011641 A) teach that an internal clock generating apparatus is provided to reduce test time by generating internal test clock pulses synchronized with both the rising and falling edges of a source clock signal, respectively (abstract, Bae et al.).

DeLisle et al. (US 5,283,889) teach that a relatively fast system control processor, such as an Intel 8051, is substituted for an Intel 8042 microprocessor in a PC/AT type compatible personal computer. In one embodiment of the invention, a System Control Processor Interface (SCPI) is provided between the central processing unit (CPU) and the system control processor (SCP) to maintain compatibility with the PC/AT bus. The combination of the faster SCP and the SCPI interface improves the overall system performance. Control circuitry is also provided for setting the A20 signal relatively quickly to allow memory access above one megabyte (abstract, DeLisle et al.).

Yutaka (JP 63134970) teaches that design data of an IC 10 consisting of a logic circuit group before inserting a scan latch is read from a fundamental data holding part 11, and the confirmation facility of existence of a fault in an input end and an output end of a circuit is calculated by a fault existence confirmation facility calculating part 12. Also, by a control facility calculating part 13, the setting facility of

a signal to the input end for confirming a fault is calculated. Subsequently, their rank order is discriminated by rank order discriminating parts 14, 15, and in order from that which is inferior inconfirmation facility, and that which is inferior in control facility, a write/read scanning circuit is inserted, and FFs 1 W8 become scan FFs. In this state, a regular scan test and a non-scan test are executed (abstract, Yutaka).

Ichiro (JP 04287510) teaches a usual flip-flop 17 acts like a usual flip-flop when an MD is zero and a scanning flip-flop 18 reaches the data load state. When the MD is '1', the scanning flip-flop 18 acts like a usual flip-flop and the usual flip-flop 17 reaches the data load state, then each clock is made independent. The test of the circuit by scanning is executed independently of the kind and state of a system clock signal (abstract, Ichiro).

The prior arts however do not teach a reset input signal for controlling reset of said flip-flops by a reset control block provided to detect a transition time of a logical level of the scan mode signal by an edge detection signal having a pulse length that is at least equal to or greater than one clock period of a system clock, wherein scan operations are inhibited without resetting at the time of initiating scan operations or normal operations without being reset upon termination of scan operations, whereby said resetting is always performed at said transition time.

Hence the prior arts of record do not anticipate nor render obvious the claimed invention. Thus, claim 41 is allowable over the prior arts of record. Claims 42-44 are allowed because of the combination of additional limitations and the limitations listed above.

- Thus, claims 24-30, 32, 33, 35-44 are allowable over the prior arts of record.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled “Comments on Statement of Reasons for Allowance.”

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DIPAKKUMAR GANDHI whose telephone number is (571)272-3822. The examiner can normally be reached on 9:00 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on (571) 272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Cynthia Britt/
Primary Examiner, Art Unit 2117

/Dipakkumar Gandhi/
Examiner, Art Unit 2117